

Please add new claims 41-110 as follows:

C 1 ~~41~~. A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a substrate;
forming a gate insulating film over said gate electrode;
depositing an amorphous semiconductor film comprising silicon on said gate insulating film;
patterning said semiconductor film into an island comprising a channel region;
forming an organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;
forming an opening in said organic leveling film; and
forming a pixel electrode over said organic leveling film through said opening, wherein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion of said opening, and wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion.

242. A method according to claim ~~41~~ further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

3 ~~42~~. A method according to claim ~~41~~ further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

44. A method according to claim 41 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

45. A method according to claim 41 wherein said gate electrode comprises aluminum.

46. A method according to claim 41 wherein said gate insulating film comprises silicon oxide.

47. A method according to claim 41 wherein said amorphous semiconductor film is deposited through plasma CVD.

48. A method according to claim 41 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

49. A method according to claim 41 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

50. A method according to claim 41 wherein said pixel electrode extends over said channel region.

51. A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;
forming a gate insulating film over said gate electrode;
depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

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patterning said semiconductor film into an island comprising a channel region;
forming a first organic leveling film over said semiconductor film after said
patterning thereof to provide a leveled upper surface;
forming an opening in said organic leveling film;
forming a pixel electrode over said organic leveling film through said opening;
forming a color filter over a second substrate;
forming a second organic leveling film over said color filter;
forming a counter electrode on said second leveling film; and
facing said second substrate to said first substrate so that said counter electrode and
said pixel electrode are opposed to each other.

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52. A method according to claim ~~51~~ further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

~~13~~
53. A method according to claim ~~51~~ further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

~~14~~
54. A method according to claim ~~51~~ wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

~~15~~
55. A method according to claim ~~51~~ wherein said gate electrode comprises aluminum.

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56. A method according to claim ~~51~~ wherein said gate insulating film comprises silicon oxide.

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~~57~~. A method according to claim ~~51~~¹¹ wherein said amorphous semiconductor film is deposited through plasma CVD.

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~~58~~. A method according to claim ~~51~~¹¹ wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

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~~59~~. A method according to claim ~~51~~¹¹ wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

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~~60~~. A method according to claim ~~51~~¹¹ wherein said pixel electrode extends over said channel region.

²¹
~~61~~. A method of manufacturing an active matrix type display device comprising the steps of:

- forming a gate electrode over an insulating surface of a first substrate;
- forming a gate insulating film over said gate electrode;
- depositing an amorphous semiconductor film comprising silicon on said gate insulating film;
- patterning said semiconductor film into an island comprising a channel region;
- forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;
- forming an opening in said organic leveling film;
- forming a pixel electrode over said organic leveling film through said opening;
- forming a resin black matrix over a second substrate;
- forming a second organic leveling film over said resin black matrix;
- forming a counter electrode on said second leveling film; and
- facing said second substrate to said first substrate so that said counter electrode and

said pixel electrode are opposed to each other.

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~~22~~
62. A method according to claim ~~61~~²¹ further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

~~23~~
63. A method according to claim ~~61~~²¹ further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

~~24~~
64. A method according to claim ~~61~~²¹ wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

~~25~~
65. A method according to claim ~~61~~²¹ wherein said gate electrode comprises aluminum.

~~26~~
66. A method according to claim ~~61~~²¹ wherein said gate insulating film comprises silicon oxide.

~~27~~
67. A method according to claim ~~61~~²¹ wherein said amorphous semiconductor film is deposited through plasma CVD.

~~28~~
68. A method according to claim ~~61~~²¹ wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

~~29~~
69. A method according to claim ~~61~~²¹ wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

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70. A method according to claim 61 wherein said pixel electrode extends over said channel region.

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71. A method of manufacturing an active matrix type display device comprising the steps of:

- forming a gate electrode over an insulating surface of a first substrate;
- forming a gate insulating film over said gate electrode;
- depositing an amorphous semiconductor film comprising silicon on said gate insulating film;
- patterning said semiconductor film into an island comprising a channel region;
- forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;
- forming an opening in said organic leveling film;
- forming a pixel electrode over said organic leveling film through said opening;
- forming a color filter over a second substrate;
- forming a resin black matrix over said second substrate;
- forming a second organic leveling film over said color filter and said resin black matrix;
- forming a counter electrode on said second leveling film; and
- facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other.

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72. A method according to claim 71 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

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73. A method according to claim 71 further comprising a step of forming a pair of

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impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

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74. A method according to claim 71 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

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75. A method according to claim 71 wherein said gate electrode comprises aluminum.

36
76. A method according to claim 71 wherein said gate insulating film comprises silicon oxide.

37
77. A method according to claim 71 wherein said amorphous semiconductor film is deposited through plasma CVD.

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78. A method according to claim 71 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

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79. A method according to claim 71 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

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80. A method according to claim 71 wherein said pixel electrode extends over said channel region.

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81. A method of manufacturing an active matrix type display device comprising the steps of:

forming a gate electrode over an insulating surface of a first substrate;

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forming a gate insulating film over said gate electrode;
depositing an amorphous semiconductor film comprising silicon on said gate insulating film;
patterning said semiconductor film into an island comprising a channel region;
forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;
forming an opening in said organic leveling film;
forming a pixel electrode over said organic leveling film through said opening;
forming a color filter over a second substrate;
forming a second organic leveling film over said color filter;
forming a counter electrode on said second leveling film; and
facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other,
wherein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion of said opening, and
wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion.

82. A method according to claim ~~81~~ further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

83. A method according to claim ~~81~~ further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

84. A method according to claim 81 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

85. A method according to claim 81 wherein said gate electrode comprises aluminum.

86. A method according to claim 81 wherein said gate insulating film comprises silicon oxide.

87. A method according to claim 81 wherein said amorphous semiconductor film is deposited through plasma CVD.

88. A method according to claim 81 wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

89. A method according to claim 81 wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

90. A method according to claim 81 wherein said pixel electrode extends over said channel region.

91. A method of manufacturing an active matrix type display device comprising the steps of:

- forming a gate electrode over an insulating surface of a first substrate;
- forming a gate insulating film over said gate electrode;
- depositing an amorphous semiconductor film comprising silicon on said gate insulating film;

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patterning said semiconductor film into an island comprising a channel region;
forming a first organic leveling film over said semiconductor film after said
patterning thereof to provide a leveled upper surface;
forming an opening in said organic leveling film;
forming a pixel electrode over said organic leveling film through said opening;
forming a resin black matrix over a second substrate;
forming a second organic leveling film over said resin black matrix;
forming a counter electrode on said second leveling film; and
facing said second substrate to said first substrate so that said counter electrode and
said pixel electrode are opposed to each other,

wherein said opening has a tapered configuration so that a diameter thereof is larger
at an upper portion than at a lower portion of said opening, and

wherein said upper portion of said opening is rounded from a first point on said
leveled upper surface of said leveling film to a second point inside said opening adjacent
said upper portion.

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92. A method according to claim 51 further comprising a step of depositing an n-
type semiconductor layer on said amorphous semiconductor film through plasma CVD using
a mixture gas containing a silane, phosphine and hydrogen.

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93. A method according to claim 51 further comprising a step of forming a pair of
impurity doped semiconductor layers on said island, wherein one of said impurity doped
semiconductor layers is electrically connected with said pixel electrode.

54
94. A method according to claim 51 wherein said gate electrode comprises a doped
silicon film and a molybdenum film formed thereon.

~~55~~ 95. A method according to claim ~~91~~ wherein said gate electrode comprises aluminum.

~~56~~ 96. A method according to claim ~~91~~ wherein said gate insulating film comprises silicon oxide.

~~57~~ 97. A method according to claim ~~91~~ wherein said amorphous semiconductor film is deposited through plasma CVD.

~~58~~ 98. A method according to claim ~~91~~ wherein said amorphous semiconductor film is deposited to a thickness of 500 to 5000 Å.

~~59~~ 99. A method according to claim ~~91~~ wherein said organic leveling film directly contacts a portion of said amorphous semiconductor film.

~~60~~ 100. A method according to claim ~~91~~ wherein said pixel electrode extends over said channel region.

~~61~~ 101. A method of manufacturing an active matrix type display device comprising the steps of:

- forming a gate electrode over an insulating surface of a first substrate;
- forming a gate insulating film over said gate electrode;
- depositing an amorphous semiconductor film comprising silicon on said gate insulating film;
- patterning said semiconductor film into an island comprising a channel region;
- forming a first organic leveling film over said semiconductor film after said patterning thereof to provide a leveled upper surface;

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forming an opening in said organic leveling film;
forming a pixel electrode over said organic leveling film through said opening;
forming a color filter over a second substrate;
forming a resin black matrix over said second substrate;
forming a second organic leveling film over said color filter and said resin black matrix;
forming a counter electrode on said second leveling film; and
facing said second substrate to said first substrate so that said counter electrode and said pixel electrode are opposed to each other,

wherein said opening has a tapered configuration so that a diameter thereof is larger at an upper portion than at a lower portion of said opening, and

wherein said upper portion of said opening is rounded from a first point on said leveled upper surface of said leveling film to a second point inside said opening adjacent said upper portion.

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102. A method according to claim 61 further comprising a step of depositing an n-type semiconductor layer on said amorphous semiconductor film through plasma CVD using a mixture gas containing a silane, phosphine and hydrogen.

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103. A method according to claim 61 further comprising a step of forming a pair of impurity doped semiconductor layers on said island, wherein one of said impurity doped semiconductor layers is electrically connected with said pixel electrode.

64
104. A method according to claim 61 wherein said gate electrode comprises a doped silicon film and a molybdenum film formed thereon.

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105. A method according to claim 61 wherein said gate electrode comprises

aluminum.

C1 ~~66~~ 106. A method according to claim ~~101~~ ⁶¹ wherein said gate insulating film comprises
Cont silicon oxide.

~~67~~ 107. A method according to claim ~~101~~ ⁶¹ wherein said amorphous semiconductor film
is deposited through plasma CVD.

~~68~~ 108. A method according to claim ~~101~~ ⁶¹ wherein said amorphous semiconductor film
is deposited to a thickness of 500 to 5000 Å.

~~69~~ 109. A method according to claim ~~101~~ ⁶¹ wherein said organic leveling film directly
contacts a portion of said amorphous semiconductor film.

~~70~~ 110. A method according to claim ~~101~~ ⁶¹ wherein said pixel electrode extends over
said channel region.--

REMARKS

The Examiner's Official Action dated August 31, 1999 has been received and its contents carefully noted. Filed concurrently herewith is a *Request for a One Month Extension of Time* which extends the shortened statutory period for response to December 21, 1999. Accordingly, applicant respectfully submits that this response is being timely filed.

Claims 21-40 were pending in the present application prior to the above amendment. Claims 21-40 have been canceled and new claims 41-110 have been added to recite additional protection to which applicant is entitled. Accordingly, new claims 41-110 are